IN THE CLAIMS:

Listing of claims:

1-12. (canceled)

13. (currently amended) A semiconductor device comprising:

tunnel insulating films, floating gates, dielectric films and control gates, all of which are laminated on first and second cell areas on a semiconductor substrate;

sources and drains formed in the first and second cell areas at positions in contact with a common plane defined by a surface of the semiconductor substrate;

a groove in the semiconductor substrate at a position between the first and second cell areas; and

a connecting area extending under the groove within the semiconductor substrate, the connecting area ~~being capable of~~ electrically connecting one of the source and drain of the first cell area with one of the source and drain of the second cell area, wherein the connecting area has an electric resistance which is lower than ~~any~~ at least one of the sources and drains of the first and second cell areas.

14. (canceled)

15. (withdrawn) The semiconductor device according to claim 13, wherein an impurity concentration of the connecting area is the same as an impurity concentration of one of the sources and drains of the first and second cell areas, and is higher than an impurity concentration of the other of the sources and drains of the first and second cell areas.

16. (currently amended) The semiconductor device according to claim 13, wherein ~~the~~ an impurity concentration of the connecting area is higher than ~~the~~ impurity concentrations of all the sources and drains of the first and second cell areas.

17. (withdrawn) The semiconductor device according to claim 13, wherein at least one

part of the connecting area has almost the same impurity depth and almost the same impurity concentration of one of a source/drain area and an off-set area of MOS transistor forming a surrounding circuit of the first and second memory cell areas.

18. (withdrawn) A circuit substrate equipped with the semiconductor device according to claim 13.

19. (withdrawn) An electronic device comprising a circuit substrate according to claim 18.

20-29. (canceled)

30. (currently amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first horizontal field effect transistor comprising a first tunnel insulating film in contact with the semiconductor substrate, a first floating gate in contact with the first tunnel insulating film, a first dielectric layer in contact with the floating gate, a first control gate in contact with the first dielectric layer, and first source/drain regions extending into the semiconductor substrate;

the second memory cell area including a second horizontal field effect transistor comprising a second tunnel insulating film in contact with the semiconductor substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the semiconductor substrate;

the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane;

a groove located in the semiconductor substrate at a position between the first and second memory cell areas; and

a connecting area ~~capable of~~ electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric

resistance which is lower than any of the first and second source/drain regions, wherein the connecting area extends under the groove in the semiconductor substrate.

31. (canceled)

32. (previously presented) The semiconductor device according to claim 30, wherein no portion of the first and second floating gates, no portion of the first and second dielectric layers, and no portion of the first and second control gates is positioned within the groove.

33. (currently amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first field effect transistor comprising a first tunnel insulating film in contact with the semiconductor substrate, a first floating gate in contact with the first tunnel insulating film, a first dielectric layer in contact with the first floating gate, a first control gate in contact with the first dielectric layer, and first source/drain regions extending into the semiconductor substrate;

the second memory cell area including a second field effect transistor comprising a second tunnel insulating film in contact with the semiconductor substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the semiconductor substrate;

a connecting area ~~capable of~~ electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the second source/drain regions, and wherein ~~the~~ an impurity concentration of the connecting area is higher than ~~the~~ impurity concentrations of the first source/drain regions and higher than ~~the~~ impurity concentrations of the second source/drain regions; and

a groove in the semiconductor substrate above at least a portion of the connecting area, wherein no portion of the first and second floating gates is positioned within the groove.

34. (previously presented) The semiconductor device according to claim 13, wherein the groove has a depth, and at least part of the connecting area has an impurity depth that is offset from that of the adjacent source/drain regions by the depth of the groove.

35. (currently amended) A semiconductor device comprising:

first and second field effect transistors spaced apart from each other, each having source/drain regions in a semiconductor substrate;

a groove extending into the semiconductor substrate at a position between the first and second field effect transistors;

the first and second field effect transistors each including a floating gate structure, wherein the floating gate structure of the first and second transistors is positioned a distance away from the groove; and

a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second field effect transistor, the conducting region being positioned below the groove and the conducting region having a lower resistance than at least one of the source/drain regions.

36. (previously presented) A semiconductor device according to claim 35, wherein the conducting region has a lower resistance than any of the source/drain regions.

37. (currently amended) A semiconductor device comprising: ~~according to claim 36,~~

first and second field effect transistors spaced apart from each other, each having source/drain regions in a semiconductor substrate;

a groove extending into the semiconductor substrate at a position between the first and second field effect transistors; and

a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second field effect transistor, the conducting region being positioned below the groove and the conducting region having a lower resistance than any of the source/drain regions;

wherein the groove has a depth, and at least part of the connecting area has an impurity

depth that is offset from that of the adjacent source/drain regions by the depth of the groove.

38. (previously presented) A semiconductor device according to claim 35, further comprising an insulating material in contact with the semiconductor substrate in the groove.

39. (currently amended) A semiconductor device comprising:

first and second memory cell means for storing data, the first and second memory cell means including source/drain regions formed in a semiconductor substrate;

a groove extending into the semiconductor substrate at a position between the first and second memory cell means; and

connecting means positioned under the groove for electrically connecting the first and second memory cell means, the connecting means having a resistance lower than that of the source/drain regions;

wherein the first and second field effect transistors each include a floating gate structure, wherein the floating gate structure of the first and second transistors is positioned a distance away from the groove.

40. (currently amended) A semiconductor device according to claim 36, further comprising an interlayer dielectric layer on the first and second field effect transistors, wherein the interlayer dielectric layer on the first and second field effect transistors also extends into the groove ~~trench~~.

41. (previously presented) A semiconductor device according to claim 36, wherein the groove comprises an etched groove having sidewalls and a lower surface.

42. (previously presented) A semiconductor device according to claim 36, wherein the groove includes sidewalls and a lower surface, wherein the sidewalls are orthogonal to the lower surface.

43. (previously presented) A semiconductor device according to claim 35, further comprising at least an insulating film above the source/drain regions, wherein at least a portion of ends of the conducting region is in direct contact with the insulating film.

44. (currently amended) A semiconductor device comprising:

tunnel insulating films, floating gates, dielectric films and control gates, all of which are laminated on first and second cell areas on a semiconductor substrate;

sources and drains formed in the first and second cell areas at positions in contact with a common plane defined by a surface of the semiconductor substrate;

a groove in the semiconductor substrate at a position between the first and second cell areas; and

an impurity area extending under the groove within the semiconductor substrate, the impurity area ~~being capable of~~ electrically connecting one of the source and drain of the first cell area with one of the source and drain of the second cell area, wherein the impurity area has an electric resistance which is lower than any one of the sources and drains of the first and second cell areas; and

wherein at least a portion of ends of the impurity area are in contact with the tunneling insulating films.

45. (previously presented) A semiconductor device according to claim 44, further comprising an interlayer dielectric layer on the control gates on the first and second cell areas, wherein the interlayer dielectric layer on the control gates also extends into the groove.

46. (previously presented) A semiconductor device according to claim 44, wherein the groove comprises an etched groove having sidewalls and a lower surface.

47. (previously presented) A semiconductor device according to claim 44, wherein the groove includes sidewalls and a lower surface, wherein the sidewalls are orthogonal to the lower surface.

48. (currently amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first field effect transistor comprising a first tunnel insulating film in contact with the semiconductor substrate, a first floating gate in contact with the first tunnel insulating film, a first dielectric layer in contact with the first floating gate, a first control gate in contact with the first dielectric layer, and first source/drain regions extending into the semiconductor substrate;

the second memory cell area including a second field effect transistor comprising a second tunnel insulating film in contact with the semiconductor substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the semiconductor substrate;

the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane;

a groove located in the semiconductor substrate at a position between the first and second memory cell areas;

an impurity area ~~capable of~~ electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the impurity area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the second source/drain regions, wherein the impurity area extends under the groove in the semiconductor substrate, wherein the impurity area also includes first and second end regions that extend adjacent to sides of the grooves; and

wherein the first end region is in contact with the first tunneling insulating film and the second end region is in contact with the second tunnel insulating film.

49. (previously presented) A semiconductor device according to claim 36, further comprising an interlayer dielectric layer on the first and second field effect transistors, wherein the interlayer dielectric layer on the first and second field effect transistors also extends into the groove.

50. (previously presented) A semiconductor device according to claim 48, wherein the groove comprises an etched groove having sidewalls and a lower surface.

51. (previously presented) A semiconductor device according to claim 48, wherein the groove includes sidewalls and a lower surface, wherein the sidewalls are orthogonal to the lower surface.

52. (previously presented) A semiconductor device according to claim 33, further comprising an interlayer dielectric layer on the first and second field effect transistors, wherein the interlayer dielectric layer on the first and second field effect transistors also extends into the groove.

53. (previously presented) A semiconductor device according to claim 33, wherein the groove comprises an etched groove having sidewalls and a lower surface.

54. (previously presented) A semiconductor device according to claim 33, wherein the groove includes sidewalls and a lower surface, wherein the sidewalls are orthogonal to the lower surface.